

Appl. No. 10/677,573  
Reply to Office Action of Nov. 3, 2004

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

1-10. (Canceled)

11. (Currently Amended) A method of forming an isolation structure in a semiconductor, comprising:  
providing a single crystal substrate;  
forming a first dielectric overlying the substrate;  
forming a second dielectric overlying the first dielectric, the second dielectric being a different material than the first dielectric;  
forming a first opening having a first diameter completely through the first dielectric and forming a second opening having a second diameter completely through the second dielectric, the second diameter being equal to or greater than the first diameter wherein the first opening and the second opening expose a surface of the single crystal substrate;  
filling the first opening and a portion of the second opening with a first single crystal semiconductor material having a relaxed state by having defects for a controlled depth from the single crystal substrate to a predetermined height, a remainder of the first single crystal semiconductor material not having defects;  
filling a remaining portion of the second opening with a second single crystal semiconductor material that is strained by having a predetermined thickness that does not exceed a critical thickness where defects begin to form; and  
forming a transistor overlying and within at least a portion of the second opening.
12. (Original) The method of claim 11 further comprising:  
forming the first opening to having a predetermined width and a predetermined depth, a ratio of the predetermined depth to the predetermined width being greater than one in order to define the controlled depth of defects of the first single crystal semiconductor material.
13. (Original) The method of claim 11 further comprising:  
using the different material of the second dielectric from the first dielectric as a control parameter to avoid excessive etching of the first dielectric and second dielectric when making electrical contact to a current electrode of the transistor.
14. (Currently Amended) The method of claim 11 further comprising:  
forming a third opening having a third diameter completely through the first dielectric and forming a fourth opening having a fourth diameter completely through the second dielectric, the

Appl. No. 10/677,573  
Reply to Office Action of Nov. 3, 2004

fourth diameter being ~~equal to or~~ greater than the third diameter wherein the third opening and the fourth opening expose the surface of the single crystal substrate; and  
filling the third opening and a portion of the fourth opening with the first single crystal semiconductor material having the relaxed state by having defects for a controlled depth from the single crystal substrate to the predetermined height, the remainder of the first single crystal semiconductor material not having defects;  
filling a remaining portion of the fourth opening with the second single crystal semiconductor material that is strained by having a predetermined thickness that does not exceed a critical thickness where defects begin to form; and  
forming a second transistor overlying and within at least a portion of the fourth opening, the second transistor being laterally adjacent the first transistor and having a current electrode directly touching a current electrode of the first transistor.

15. (Currently Amended) The method of claim 11 further comprising:  
forming a third opening having a third diameter completely through the first dielectric and forming a fourth opening having a fourth diameter completely through the second dielectric, the fourth diameter being ~~equal to or~~ greater than the third diameter wherein the third opening and the fourth opening expose the surface of the single crystal substrate; and  
filling the third opening and a portion of the fourth opening with the first single crystal semiconductor material having the relaxed state by having defects for a controlled depth from the single crystal substrate to the predetermined height, the remainder of the first single crystal semiconductor material not having defects;  
filling a remaining portion of the fourth opening with a fourth single crystal semiconductor material that is strained by having a predetermined thickness that does not exceed a critical thickness where defects begin to form; and  
forming a second transistor overlying and within at least a portion of the fourth opening, the second transistor being laterally adjacent the first transistor but not directly electrically connected to the first transistor.
16. (Currently Amended) A method of forming an isolation structure in a semiconductor, comprising:  
providing a single crystal substrate;  
forming a dielectric overlying the single crystal substrate;  
forming a first opening having a first diameter through a portion of the dielectric and forming a second opening having a second diameter through a remainder of the dielectric, the second diameter being ~~equal to or~~ greater than the first diameter wherein the first opening and the second opening expose a surface of the single crystal substrate;

Appl. No. 10/677,573  
Reply to Office Action of Nov. 3, 2004

- filling the first opening and a portion of the second opening with a first single crystal semiconductor material having a relaxed state by having defects for a controlled depth from the single crystal substrate to a predetermined height, a remainder of the first single crystal semiconductor material not having defects;
- filling a remaining portion of the second opening with a second single crystal semiconductor material that is strained by having a predetermined thickness that does not exceed a critical thickness where defects begin to form; and
- forming a transistor overlying and within at least a portion of the second opening.
17. (Original) The method of claim 16 further comprising:
- forming the first opening to having a predetermined width and a predetermined depth, a ratio of the predetermined depth to the predetermined width being greater than one in order to define the controlled depth of defects of the first single crystal semiconductor material.
18. (Currently Amended) The method of claim 16 further comprising:
- forming a third opening having a third diameter through a second portion of the dielectric and forming a fourth opening having a fourth diameter through a remainder of the second portion of the dielectric, the fourth diameter being ~~equal to or~~ greater than the third diameter wherein the third opening and the fourth opening expose the surface of the substrate;
- filling the third opening and a portion of the fourth opening with the first single crystal semiconductor material having the relaxed state by having defects for a controlled depth from the single crystal substrate to the predetermined height, the remainder of the first single crystal semiconductor material not having defects;
- filling a remaining portion of the fourth opening with the second single crystal semiconductor material that is strained by having a predetermined thickness that does not exceed a critical thickness where defects begin to form; and
- forming a second transistor overlying and within at least a portion of the fourth opening, the second transistor being laterally adjacent the first transistor and having a current electrode directly touching a current electrode of the first transistor.
19. (Currently Amended) The method of claim 16 further comprising:
- forming a third opening having a third diameter through a second portion of the dielectric and forming a fourth opening having a fourth diameter through a remainder of the second portion of the dielectric, the fourth diameter being ~~equal to or~~ greater than the third diameter wherein the third opening and the fourth opening expose the surface of the substrate;
- filling the third opening and a portion of the fourth opening with the first single crystal semiconductor material having the relaxed state by having defects for a controlled depth

Appl. No. 10/677,573  
Reply to Office Action of Nov. 3, 2004

from the single crystal substrate to the predetermined height, the remainder of the first single crystal semiconductor material not having defects;  
filling a remaining portion of the fourth opening with the second single crystal semiconductor material that is strained by having a predetermined thickness that does not exceed a critical thickness where defects begin to form; and  
forming a second transistor overlying and within at least a portion of the fourth opening, the second transistor being laterally adjacent the first transistor but not directly electrically connected to the first transistor.

20. (Original) The method of claim 18 further comprising:  
forming the first single crystal material with silicon germanium;  
forming the second single crystal material with silicon;  
forming the single crystal substrate with silicon; and  
forming the dielectric with one of silicon dioxide or silicon nitride.